A High Performance CCD on High Resistivity Silicon

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ABSTRACT

In this paper we present new results from the characterization of a fully depleted CCD on high resistivity silicon. The CCD was fabricated at Lawrence Berkeley National Laboratory on a 10-12 KΩ-cm n-type silicon substrate. The CCD is a 200X200 15-μm square pixel array. The high resistivity of the starting material makes it possible to deplete the entire 300 μm thick substrate. This results in improved red and near infrared response compared to a standard CCD. Because the substrate is fully depleted, thinning of the CCD is not required for backside illumination, and the results presented here were obtained with a backside illuminated device. In this paper we present measured quantum efficiency as a function of temperature, and we describe a novel clocking scheme to measure serial charge transfer efficiency. We demonstrate an industrial application in which the CCD is more than an order of magnitude more sensitive than a commercial camera using a standard CCD.

Keywords: CCD, high resistivity, fully depleted, Lick Observatory, Lawrence Berkeley National Laboratory, astronomical

2. INTRODUCTION

The CCD described here was developed for astronomical imaging applications. However, the device characteristics give it many advantages over a standard CCD and therefore it should have potential benefits for other remote sensing applications. The design and fabrication of these devices is described by Holland *et.al*,[1] and initial test results are presented by Stover *et.al*[2]. These CCDs are based on work done at Lawrence Berkeley National Laboratory to develop fully-depleted p-i-n diodes for high-energy physics applications, and all design and fabrication work on the CCDs was carried out there. The starting material for these devices is approximately 10,000 Ω-cm float-zone refined n-type silicon, in 300 μm thick wafers. The CCD employs 15 μm square pixels in a 200x200 array. Standard triple-poly MOS processing was used in fabrication. All testing and characterizations were carried out in the Detector Development Laboratory of the University of California Observatories/Lick Observatory (UCO/Lick) in Santa Cruz, using the standard UCO/Lick data acquisition system[3].

Scientific CCDs have traditionally been fabricated on highly doped p-type silicon, with an active thickness of 25 μm or less. This results in several performance limitations:

1. Illuminated from the front side, quantum efficiency is reduced at all wavelengths by reflections from the polysilicon gate structures.
2. At the blue end of the visible spectrum quantum efficiency for frontside illumination drops to near zero due to absorption in the polysilicon gates.

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3. For red wavelengths (λ > 750 nm) quantum efficiency drops rapidly because absorption pathlength in silicon becomes large compared to the active thickness of the device.

To overcome the loss of quantum efficiency due to the gate structures on the front of the CCD, the traditional CCD can be thinned to about 20 μm and illuminated from the backside. Excellent results have been achieved with this method. However, the thinning process is difficult and expensive, and the thinned CCD does not improve quantum efficiency in the red. In fact, the thinned CCD starts to become transparent at λ > 750 nm, and high-order interference fringes are produced by multiply-reflected waves. The accurate calibration of this effect is one of the primary limitations in astronomical imaging at these wavelengths. In p-type silicon the photo-generated electrons tend to be attracted to, and trapped by, the backside surface. Additional processing to modify the backside potential is required to help minimize this problem.

The CCD described here overcomes all of these limitations. Backside illumination is possible without thinning because we can deplete the entire 300 μm thickness of the silicon wafer. With this thickness excellent red response is possible with λ > 1000nm and interference fringes are eliminated. Because the CCD is fabricated on n-type silicon, holes are the signal carrier, and electron trapping at the backside surface is not a problem.

3. LABORATORY CHARACTERIZATIONS

3.1 Quantum efficiency

The back surface of a thinned p-type silicon CCD naturally develops a potential that attracts and traps photogenerated charge. As a result a newly thinned p-type CCD exhibits very low quantum efficiency. Various processes have been developed to modify the backside surface potential to help reduce the trapping of charge. However, if charge trapping is not eliminated completely, then the quantum efficiency (QE) of the CCD can exhibit instabilities due to a variety of environmental factors including device operating temperature. If this occurs, the QE typically drops as the device temperature is lowered. Since astronomical imaging often requires long exposures on faint sources of light, cooling to about -120^{o}C is required to reduce thermally generated electrons, and it becomes important to maintain high QE when cooled to this temperature.

Since our n-type CCD does not have the problem of charge trapping at the backside surface, we expected better QE stability than is often seen in p-type silicon CCDs. To verify this behavior we measured QE at 10-degree intervals between -90^{o}C and -130^{o}C. Quantum efficiency was measured through a series of narrow-band interference filters, using a calibrated UDT Sensors, Inc. Model PIN UV 100 silicon photodiode as a reference. The results of those measurements are shown in Figure 1. Because there was essentially no QE variation with temperature, we have averaged the measurements at each wavelength and the averages are given in Table 1.

λ (nm)	**QE (%)**
320	21.3
350	32.4
400	66.7
450	77.7
500	85.7
600	81.7
650	79.4
700	78.0
800	73.4
900	70.7
1000	50.4

TABLE 1. Average measured QE from a series of measurements between -90^{o}C and -130^{o}C.

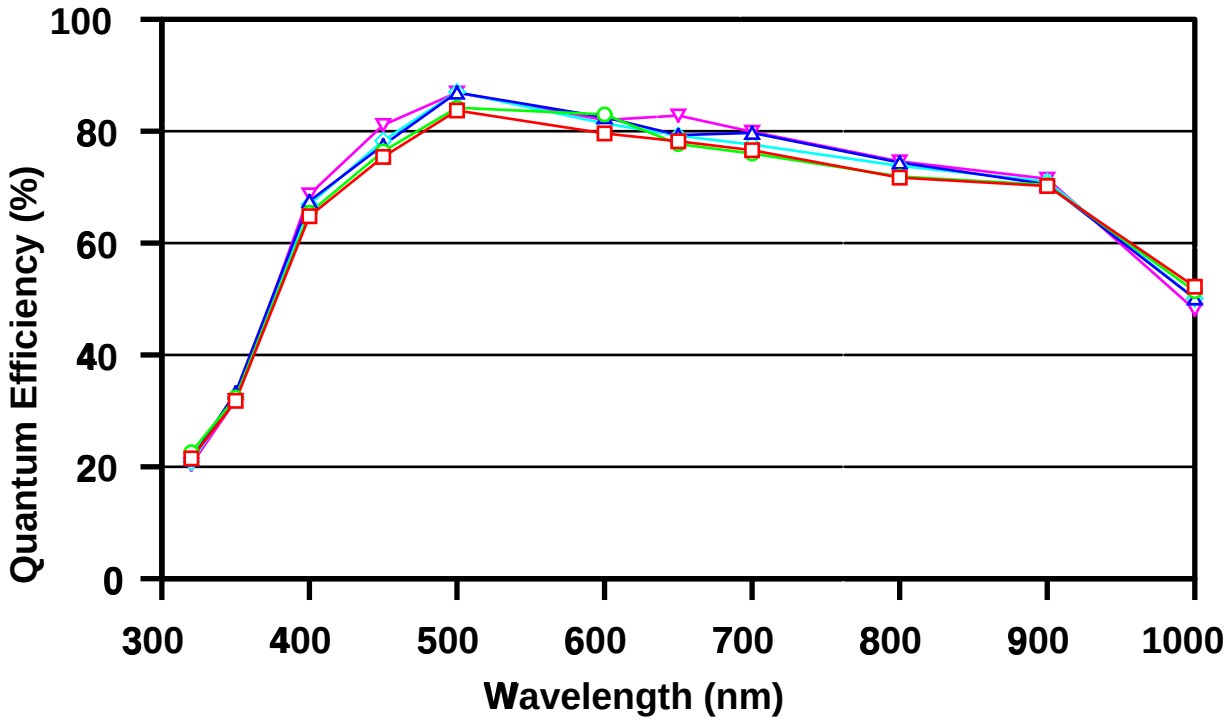

FIGURE 1. Measured quantum efficiency at five temperatures between -90°C and -130°C. N-type silicon has inherent QE stability, as this figure illustrates.

3.2 Charge Transfer Efficiency

The traditional method for measuring charge transfer efficiency (CTE) is to expose the CCD to x-rays from Fe^{55} or a similar source. Each absorbed x-ray produces a charge packet of known size. By analyzing an image of x-ray events it is possible to measure the amount of charge lost in each event. Comparing this charge loss to the number of transfers required to read each event yields the charge transfer efficiency. It is relatively easy to measure 1% charge losses with this method. But with only 200 rows and 200 columns a 1% loss translates into a CTE of 0.99995, which is not very good by modern scientific CCD standards. Because our CCD clearly exhibits better CTE than this, the traditional method is not sensitive enough to yield a reliable measure of CTE. Therefore we developed a new CCD clocking scheme to increase the effective size of the CCD serial register and to measure serial CTE.

We first make an exposure with uniform illumination. One row is transferred into the CCD serial register and then the serial clocks are run to discard all of the image pixels except the last pixel. This single pixel is then shifted back toward the center of the serial register. Next the serial clocks are run to shift the single pixel of charge back and forth in the register many times. Finally, the charge is shifted out of the serial register in normal fashion, amplified, and digitized. The next row is shifted into the serial register and read out in normal serial-clocking fashion. The sequence of special-clocking row and normal-clocking row is repeated 100 times, until the entire CCD is read out. The normal-clocking rows provide an accurate calibration on the original charge level while the 100 special-clocking rows provide data on charge transfer efficiency of the single pixel of charge. To improve the signal-to-noise ratio we may average together up to 10 images before analyzing the results. Analysis of the results is somewhat more complex than the traditional x-ray method because the charge is swept back and forth many

times over the same part of the serial register. If charge is lost while shifting in one direction, it may be picked up again while shifting in the opposite direction. If low-level CTE is different from high-level CTE additional complications can occur. However, all of these effects are simple to model, and an accurate CTE measurement is possible.

Our CTE clocking scheme allows us to sample the CTE at various locations on the serial register by selecting where the single pixel of charge will be placed before the back and forth charge shifting occurs. Using this technique we have found some sections of the serial register which exhibit near perfect CTE (at least 0.999999) and one section with somewhat lower, but still good CTE. This lower CTE might represent a single pixel with a very slight charge-trapping problem, but in our tests we shifted the charge back and forth 20 pixels, so we can't resolve individual pixel locations. We further investigated CTE as a function of signal level. We found that the near perfect sections of the serial register were uniformly excellent at all signal levels. The section with lower CTE exhibited variations with signal level, and that variation is shown in Figure 2. All of our measurements were made at a temperature between -120^{o}C and -130^{o}C.

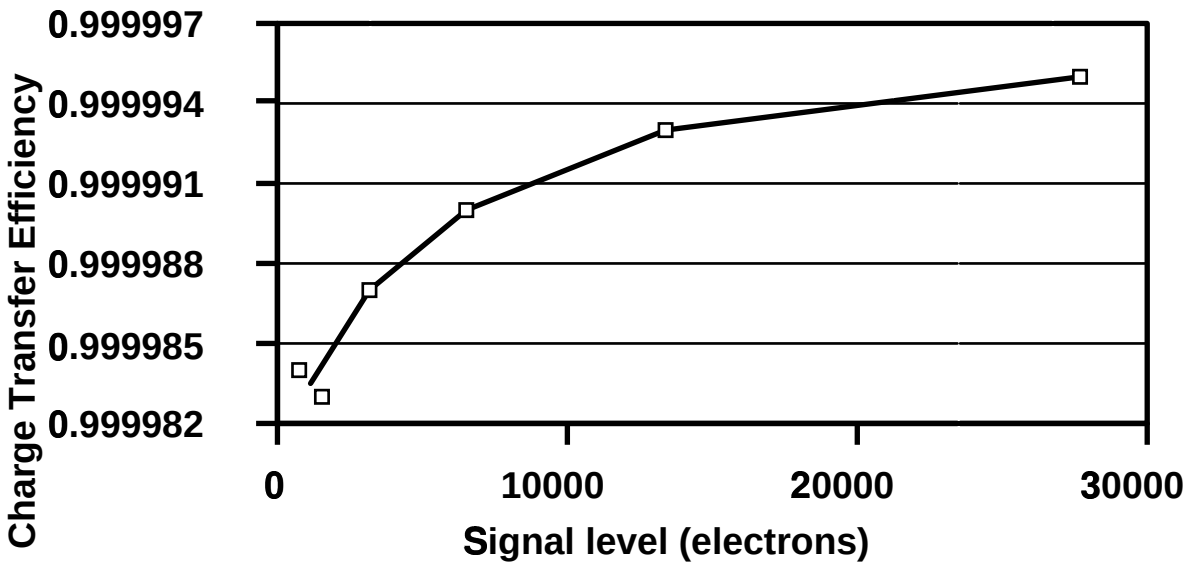

FIGURE 2. CTE is shown as a function of signal level for one section of the CCD serial register.

Note that the CTE shown in Figure 2 is still very good and occurs in one small section of the serial register. This probably would not even be noticed using the traditional x-ray method for measuring CTE.

3.3 Industrial Monitoring Application

We have been working with an integrated circuit manufacturer on an application of the high-resistivity CCD which takes advantage of its excellent response in the near infrared part of the spectrum. In this application we are imaging an integrated circuit which is normally mounted face-down so that none of the components of the integrated circuit are visible at optical wavelengths. To monitor the operation of the device we image the light emissions from various junctions on the integrated circuit. Only those wavelengths that can pass through the 500 μm thick substrate emerge from the integrated circuit. However, because of the good QE of the high-resistivity CCD, we are able to image these emissions relatively easily. Figure 3 shows three frames of the same integrated circuit under various operating conditions. The frame on the left shows the typical pattern of emissions after the device is first powered up. The middle frame shows the pattern of emissions when the circuit's "chip select" signal is de-asserted. The right frame shows the emissions when "chip select" is re-asserted. Had this been a properly

functioning device the left and right frames would look identical. In fact they do not, and the difference between the two frames gives the integrated circuit design engineers valuable clues as to why this device is not working.

The circuit manufacturer tried this same experiment using a commercial camera with a standard scientific CCD. He estimates that the high-resistivity CCD is at least forty (40) times faster than the CCD in his commercial camera. This increase in sensitivity greatly reduces the time required to examine a single circuit, and the reduced exposure time makes it practical to check every device on the production line.

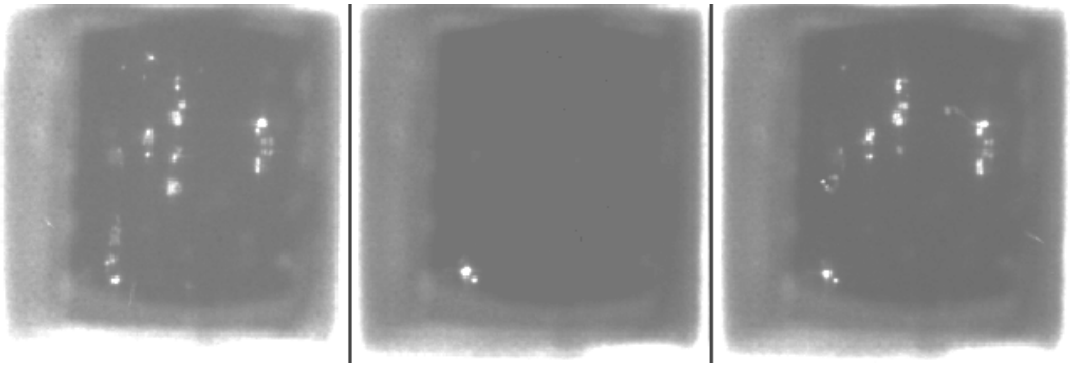

FIGURE 3. Three frames of the same integrated circuit, showing infrared emissions from the device. The pattern of emissions can be used to verify proper operation or to provide valuable clues for diagnosing problems.

4. CONCLUSIONS

We have shown that the quantum efficiency of the high-resistivity CCD is very stable as the temperature of the device is reduced to the typical operating temperature of -120^{o}C. This QE stability should relax the temperature stability requirements for operation of these devices in astronomical instruments and may eliminate the need for an active temperature control system.

We have developed a new clocking scheme that allows us to measure CTE, and we have measured CTE in the serial register of the high-resistivity CCD as high as 0.999999. For one region of the serial register we have measured CTE as a function of signal level. This is a measurement that can't be done with the typical x-ray illumination method because the x-ray method produces a single-size charge packet for each absorbed x-ray.

We have demonstrated an industrial imaging application of the high-resistivity CCD. The application, imaging of the infrared light emissions from an integrated circuit, takes advantage of the CCD's high QE in the near infrared. Compared to a camera equipped with a standard scientific CCD, the high-resistivity CCD camera is at least 40 times faster, making it suitable for real-time monitoring.

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